CLAIMS

What is claimed is:

1. An integrated video distribution system for distributing video signals from a plurality of sources, comprising:

a control bus;

a video digitizer arrangement coupled to the control bus and having a plurality of analog video input ports and a plurality of digital video output ports, the digitizer arrangement configured and arranged to convert analog video signals to digital video data in YCrCb format at a first clock rate, each output port coupled to a respective first set of signal lines;

a video data multiplexer arrangement having input ports coupled to output ports of the video digitizer arrangement, the multiplexer arrangement having a plurality of output ports, each coupled to a respective second set of signal lines, the multiplexer configured and arranged to multiplex the digital video data at a second clock rate that is less than the first clock rate, wherein a number of signal lines in each first set is greater than a number of signal lines in each second set;

a digital video bus having a plurality of video channels coupled to respective output ports of the multiplexer, wherein each channel carries a stream of video data; and

a plurality of terminal controllers responsive to an input signal coupled to the video bus and to the control bus, each terminal controller having a data input port and a video output port and configured and arranged to select a subset of the streams of video data for output.

2. The system of claim 1, wherein the control signal is received at the terminal controller via the input port.

3. The system of claim 1, further comprising a backplane arrangement including the video bus and the control bus and having a plurality of expansion slots for connecting to the terminal controllers, each slot having pins coupled to the video bus and to the control bus.

4. The system of claim 1, further comprising a fail-safe video subsystem having a plurality of video signal input ports and a plurality of output ports, wherein selected ones of

the input ports are coupled to output ports of the terminal controllers, and others of the input ports are arranged to be coupled to alternative video sources, wherein the fail-safe video subsystem is configured and arranged to provide on the output ports video signals from the alternative video sources in absence of power to the fail-safe video subsystem.

5. The system of claim 4, wherein the fail-safe video subsystem is comprised of a plurality of stations, wherein selected ones of the stations include:

a first relay having first and second output terminals and an input terminal arranged to be coupled to an associated one of the alternative video sources, wherein the first relay connects the input terminal to the first output terminal when in an energized state and connects the input terminal to the second output terminal when in a non-energized state;

a multiplexer having an output port, a first input port coupled to an associated one of the terminal controllers, and a second input port coupled to the first output terminal of the first relay; and

a second relay having a first input terminal coupled to the output port of the multiplexer, a second input terminal coupled to the second output terminal of the first relay, and an output terminal coupled to an output port of the fail-safe video subsystem, wherein the second relay connects the first input terminal to the output terminal when in an energized state and connects the second input terminal to the output terminal when in a non-energized state.

6. The system of claim 4, wherein the digitizer arrangement further comprises:

a plurality of digitizers coupled to the analog video input ports;

a plurality of digital video receivers having input ports arranged to receive input digital video signals, respectively; and

a video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus.

7. The system of claim 6, wherein the video bus controller arrangement is implemented with one or more field programmable gate arrays (FPGAs).

8. The system of claim 7, further comprising:

a first FPGA having input ports coupled to output ports of the digitizers, the first FPGA configured and arranged to multiplex digitized video signals generated from video signals from the analog video input ports over the video channels of the video bus; and

a second field programmable gate array having input ports coupled to output ports of the video receivers, the second FPGA configured and arranged to multiplex the input digital video signals over the video channels of the video bus.

9. The system of claim 6, wherein the video channels are comprised of a first set and a second set of video channels, each channel of the first set having a number of signal lines sufficient for parallel transmission of multiple streams of monochrome video data, and each channel of the second set having a number of signal lines sufficient for transmission of a single stream of color video data.

10. The system of claim 4, further comprising:

a plurality of display terminals coupled to the terminal controllers, respectively; and

a plurality of input devices coupled to the terminal controllers, respectively, the input devices arranged for input of control signals to the terminal controllers to select certain ones of the video signals for display at the display terminals.

11. The system of claim 10, wherein the input device is a point-and-click device.

12. The system of claim 10, wherein the input device includes a touchscreen.

13. The system of claim 1, wherein the digitizer arrangement further comprises:

a plurality of digitizers coupled to the analog video input ports;

a plurality of digital video receivers having input ports arranged to receive input digital video signals, respectively; and

a video bus controller arrangement having data input ports coupled to the digitizers and to the video receivers, the video bus controller configured and arranged to multiplex the video signals over the video channels of the video bus.

14. The system of claim 13, wherein the video bus controller arrangement is implemented with one or more field programmable gate arrays (FPGAs).

15. The system of claim 14, further comprising:

a first FPGA having input ports coupled to output ports of the digitizers, the first FPGA configured and arranged to multiplex digitized video signals generated from video signals from the analog video input ports over the video channels of the video bus; and

a second field programmable gate array having input ports coupled to output ports of the video receivers, the second FPGA configured and arranged to multiplex the input digital video signals over the video channels of the video bus.

16. The system of claim 14, wherein the video channels are comprised of a first set and a second set of video channels, each channel of the first set having a number of signal lines sufficient for parallel transmission of multiple streams of monochrome video data, and each channel of the second set having a number of signal lines sufficient for transmission of a single stream of color video data.

17. The system of claim 1, further comprising:

a plurality of display terminals coupled to the terminal controllers, respectively; and

a plurality of input devices coupled to the terminal controllers, respectively, the input devices arranged for input of control signals to the terminal controllers to select certain ones of the video signals for display at the display terminals.

18. The system of claim 17, wherein the input device is a point-and-click device.

19. The system of claim 18, wherein the input device includes a touchscreen.

20. The system of claim 1, wherein the second clock rate is about half of the first clock rate.

21. The system of claim 20, wherein the video data multiplexer arrangement generates data that defines a color pixel, each pixel defined by at least four words of data and a color video control code.

22. The system of claim 21, wherein a first data word and a third data word of the four data words are transmitted on a rising clock edge and a second data word and a fourth data word are transmitted on a falling clock edge at the second clock rate.

23. The system of claim 22, wherein the first and second data words define chroma red data, the third and fourth data words define chroma blue data, and all four data words define luma data for the color pixel.

24. The system of claim 23, wherein the data words are clocked at a frequency of 33MHz.

25. The system of claim 20, wherein the video data multiplexer arrangement generates data that defines a monochrome pixel, each pixel defined by a set of data words and a monochrome video control code.

26. The system of claim 25, wherein a first data word is transmitted on a rising clock edge and a second data word is transmitted on a falling clock edge at the second clock rate.

27. A method for distributing video signals from a plurality of sources, the method comprising:

inputting a plurality of analog video signals;

digitizing the plurality of analog video signals to respective streams of digital video data in YCrCb format at a first clock rate and outputting the digital video data on a first plurality of sets of signal lines;

multiplexing the digital video data at a second clock rate and outputting the digital video data on a second plurality of sets of signal lines, wherein the second clock rate is less than the first clock rate and a number of signal lines in each set of the first plurality is greater than a number of signals in each set of the second plurality; and

selecting one or more of the streams of video data for output responsive to an input control signal and converting the selected streams of video data to analog video signals.

28. The method of claim 27, wherein the step of multiplexing the digital video data includes generating data that defines a pixel with a set of data and a video control signal.

29. The method of claim 28, wherein the step of generating multiplexed data includes transmitting a first data word and a third data word on a rising clock edge and transmitting a second data word and a fourth data word on a falling clock edge at the second clock rate for a color pixel.

30. The method of claim 28, wherein the step of generating multiplexed data includes transmitting a first data word on a rising clock edge and transmitting a second data word on a falling clock edge at the second clock rate for a monochrome pixel.

31. An integrated video distribution arrangement for distributing video signals from a plurality of sources, the arrangement comprising:

means for inputting a plurality of analog video signals;

means for digitizing the plurality of analog video signals to respective streams of digital video data in YCrCb format at a first clock rate and outputting the digital video data on a first plurality of sets of signal lines;

means for multiplexing the digital video data at a second clock rate and outputting the digital video data on a second plurality of sets of signal lines, wherein the second clock rate is less than the first clock rate and a number of signal lines in each set of the first plurality is greater than a number of signals in each set of the second plurality; and

means for selecting one or more of the streams of video data for output responsive to an input control signal and converting the selected streams of video data to analog video signals.